Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of claims:

1. (Currently Amended) A processor comprising:

means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size; and

means for confining the application to a first bit size address space subset, said means for confining comprising:

means for truncating generated address references of the second bit size to the first bit size;

means for determining that the first bit size address space subset is signed address space or unsigned address space based on a setting of an address format control signal, the address format control signal having a first setting to indicate unsigned address space and a second setting to indicate signed address space; and

means for extending to the second bit size the truncated generated address references based ~~at least in part~~ on results from said means for determining, zero-extending the truncated generated address references if the first bit size address space subset is unsigned and sign-extending the truncated generated address references if the first bit size address space subset is signed ~~a setting of an address format control signal a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references.~~

2. (Original) The processor of claim 1, wherein the first bit size is 32-bit and the second bit size is 64-bit.

3. (Cancelled)

4. (Previously Presented) The processor of claim 1, wherein the means for confining includes means for generating an address fault.

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) A processor comprising:

a memory to store an instruction of an application ported from a first bit size environment to a second bit size environment, the second bit size being greater than the first bit size; and

an instruction execution core coupled to said memory, said instruction execution core to execute the instruction of the application, said instruction execution core to

determine that the application is confined to a first bit size address space subset;

generate an address reference of the second bit size as part of execution of the instruction;

truncate the generated address reference from the second bit size to the first bit size;

determine that the first bit size address space subset is signed address space or unsigned address space based on a setting of an address format control flag, the address format control flag having a first setting to indicate unsigned address space and a second setting to indicate signed address space;

zero extend the truncated, generated address reference to the second bit size if the first bit size address space subset is determined to be unsigned address space; and

sign extend the truncated, generated address reference ~~from the first bit size~~ to the second bit size if the first bit size address space subset is determined to be signed address space ~~based at least in part on a setting of an address format control signal, a first setting~~

~~of the address format control signal to indicate zero-extension of the truncated generated address reference and a second setting of the address format control signal to indicate sign-extension of the truncated generated address reference~~.

8. (Original) The processor of claim 7, wherein the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment.

9. (Previously Presented) The processor of claim 7, wherein the instruction execution core is to determine that the application is confined to a first bit size address space subset based at least in part on an address space control flag.

10. (Cancelled)

11. (Previously Presented) The processor of claim 7, wherein the instruction execution core is to generate an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference.

12. (Currently Amended) The processor of claim 11, wherein the instruction execution core is to generate ~~an~~ the address fault flag only if:

the comparison of the generated address reference and the extended, truncated, generated address reference indicates that the compared addresses are different, and

~~based at least in part on~~ an address fault control flag specifies to check for an address fault.

13. (Original) The processor of claim 7, wherein said memory is a cache memory.

14. (Original) The processor of claim 7, wherein the processor is a 64-bit processor.

15. (Currently Amended) A method comprising:

determining that an application is confined to a first bit size address subset, the application including an instruction;

generating an address reference of a second bit size as part of execution of the instruction;

truncating the generated address reference from the second bit size to the first bit size;

determining that the first bit size address space subset is signed address space or unsigned address space based on a setting of an address format control flag, the address format control flag having a first setting to indicate unsigned address space and a second setting to indicate signed address space;

zero-extending the truncated, generated address reference to the second bit size if the first bit size address space subset is determined to be unsigned address space; and

sign-extending the truncated, generated address reference ~~from the first bit size~~ to the second bit size if the first bit size address space subset is determined to be signed address space ~~based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address reference and a second setting of the address format control signal to indicate sign-extension of the truncated generated address reference~~.

16. (Cancelled)

17. (Previously Presented) The method of claim 15, wherein the application is ported from a 32-bit environment to a 64-bit environment.

18. (Currently Amended) The method of claim 15, wherein said determining that ~~an~~ the application is confined to [[a]] the first bit size address subset~~, the application including an instruction that~~ is based at least in part on an address space control flag.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Currently Amended) The method of claim 15, further comprising:

~~wherein extending the truncated, generated address reference from the first bit size to the second bit size includes~~ generating an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference.

23. (Currently Amended) The method of claim 22, wherein generating ~~an~~ the address fault flag is further based ~~at least~~ in part on an address fault control flag, wherein the address fault flag is generated only if:

the comparison of the generated address reference and the extended, truncated, generated address reference indicates that the compared addresses are different, and

an address fault control flag specifies to check for an address fault.

24. (New) The processor of claim 4, wherein said means for generating the address fault comprises:

means for comparing a generated address reference as input into said means for truncating with an extended, truncated, generated address reference as output by said means for extending,

wherein said means for generating the address fault outputs that an address fault has occurred only if:

an output of said means for comparing indicates that the compared addresses are different, and

an address fault control signal specifies to check for the address fault.